# BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY

Mangalpally (Village), Ibrahimpatnam (Mandal), Ranga Reddy (District), Telangana-501510

## 1.3.3 : Percentage of students undertaking project work/ field work / internship (Data for the latest completed academic year) (10)

## Academic Year 2018-19

| S. No. | Department | Descriptions | Total Count |
|---|---|---|---|
| 1. | B.Tech-CIVIL | Major Project Work | 74 |
| 2. | B.Tech-EEE | Major Project Work | 116 |
| 3. | B.Tech-MECHANICAL | Major Project Work | 72 |
| 4. | B.Tech-ECE | Major Project Work | 161 |
| 5. | B.Tech-CSE | Major Project Work | 222 |
| 6. | B.Tech-IT | Major Project Work | 43 |
| 7. | MBA | Major Project Work | 10 |
| 8. | M.TECH | Major Project Work | 19 |
| 9. | B.Tech-(CIVIL, EEE, MECHANICAL, ECE, CSE)<br>MBA | Internship | 134 |
| 10. | B.Tech-(EEE, MECHANICAL,ECE, CSE, 1ST YEAR STUDENTS)<br>MBA, | Industrial visit | 693 |
| TOTAL COUNT | | | 1544 |

BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY
Mangalpally(V), Ibrahimpatnam, R R District E1

**PRINCIPAL**

Principal
Bharat Institute of Engg. and Tech
Mangalpally(V), Ibrahimpatnam(M)
Ranga Reddy (Dist)-Telangana-501510

# BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY
## ACADEMIC YEAR:2018-19
## MAJOR PROJECTS :GUIDE ALLOCATION LIST
## M.tech-CSE

| S.No | Student Name | H.No | Thesis Title |
|---|---|---|---|
| 1 | A.SANDHYA | 17E11D5801 | ENABLING CLOUD STORAGE AUDITING WITH VERIFIABLE OUTSOURCING OF KEY UPDATES |
| 2 | L.PRASANNA LAXMI | 17E11D5805 | ANAMOLY BASED FINANCIAL FRAUD AND FEATURE DETECTION |
| 3 | RAVULA ANITHA | 17E11D5809 | BRANCH COVERAGE TECHNIQUES RETAINING TEST CASES |
| 4 | SAPAVATH RAJITHA | 17E11D5811 | SECURE OVER LARGE SCALE INFORMATION DIFFERENTIAL DATA ITEMS EXTREME |

# BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY
## ACADEMIC YEAR:2018-19
## MAJOR PROJECTS :GUIDE ALLOCATION LIST
## EPE-EEE DEPARTMENT

| S.No | Student Name | H.No | Thesis Title |
|---|---|---|---|
| 1 | **P MANISH KUMAR** | 17E11D4901 | **IMPROVEMENT OF RESILIENCE OF AN EXISTENCE OF MICRO GRID USING FRAGILITY MODELLING AND SIMULATION** |
| 2 | **MR.** A. NIKITHA | 17E11D4902 | **GRID CONNECTED PHOTO VOLTAIC SYSTEM CONTROL STRATEGY AND SUPPRESS HARMONICS OF MICRO GRID** |
| 3 | **D.MANASA** | **17E11D4906** | **IMPROVED FUZZY CONTROLLED PV WIND BASED MICROGRID WITH PQ FEATURES** |
| 4 | **P. HARIKA** | **17E11D4909** | **IMPROVEMENT OF PQ USING DVR BY DIFFERENT CONTROL TECHNIQUES** |
| 5 | **T SHALINI** | **17E11D4905** | **IMPROVEMENT OF POWER QUALITY BY MULTILEVEL INVERTER BASED UPQC USING PI & FUZZY CONTROLLERS** |
| 6 | **B MAHESH** | **17E11D4910** | **REDUCING HARMONICS IN MICRO GRID DISTRIBUTION USING APF WITH FUZZY LOGIC CONTROLLER** |
| 7 | **MASANNAPETA RAJU** | **17E11D4907** | **AN EFFICIENT HYBRID CONTROLLER FOR PV CONNECTED GRID SYSTEM WITH IMPROVED POWER QUALITY** |

# BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY

## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

**WMC ACADEMIC YEAR:2018-19**

| SNO | ROLL NO | STUDENT NAME | PROJECT TITLE | Guide Name |
|---|---|---|---|---|
| 1 | 16E11D6501 | SNEHA MERIN PHILIP | High Performance of 5G systems using massive mimo | Dr. NAVEEN RATHE |
| 2 | 16E11D6502 | SAI BHARGAV | Advanced Co-Existence system of long term evolution relavances | Dr. Rambabu Vatti |
| 3 | 16E11D6503 | SUKUMAR REDDY | Identifying data interchange for cognitive radio networks through clamor inconsistency insecurity | Dr. K. S. BALAMURUGAN |

# BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

**ACADEMIC YEAR:2018-19**

**MTECH R17 BATCH ECE DEPART. VLSI SYSTEM DESIGN PROJECT TITLES WITH GUIDE NAME**

| SNO | ROLL NO | STUDENT NAME | PROJECT TITLE | Guide Name |
|---|---|---|---|---|
| 1 | 16E11D6505 | k Gouthami | Modern Data transmission for vehicular networks with cooperative schemes | Dr. Naveen Rathe |
| **2** | 17E11D5706 | GOGIREDDY PAVANI | Implementation of 4-bit Vedic Multiplier. | Mr. Basavaraj |
| 3 | 17E11D5709 | Reddigari Shashikala | VLSI Implementation of High Performance of Arthimetic circuits | D Shankar Reddy |
| 4 | 17E11D5711 | THADAKALA RANJITH I | Timing Analysis of Discontinuous Rc inetrconnect Lines | Dr. Naveen Rathe |
| 5 | 16E11D5712 | Mah Jabeen | Design and Implimentation of Majority logic of parallel using adders cogge stone adder for reducing circuit complexcity using FPGA | V Pradeep Kumar |

# ENABLING CLOUD STORAGE AUDITING WITH VERIFIABLE OUTSOURCING OF KEY UPDATES

*A Project Report Submitted to*

**Jawaharlal Nehru Technological University Hyderabad**

*In partial fulfillment of the requirements*
*for the award of the degree of*

**MASTER OF TECHNOLOGY**
**IN**
**COMPUTER SCIENCE AND ENGINEERING**

*By*

**ANNEVENA SANDHYA** **(17E11D5801)**

*Under the guidance of*

**Dr. R. DELSHI HOWSALYA DEVI**

Associate Professor

**DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING**
**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**
(Affiliated to JNTUH Hyderabad, Approved by AICTE and Accredited by NBA)
Ibrahimpatnam - 501 510, Hyderabad

**2019 - 2020**

**DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING**

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**

(Affiliated to JNTUH Hyderabad, Approved by AICTE and Accredited by NBA)
Ibrahimpatnam - 501 510, Hyderabad

# *Certificate*

*This is to certify that the project work entitled "**Enabling Cloud Storage Auditing With Verifiable Outsourcing Of KeY Updates**" is the bonafide work done*

**By**

**ANNEVENA SANDHYA (17E11D5801)**

*in the Department of Computer Science and Engineering, **BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**, Ibrahimpatnam is submitted to **Jawaharlal Nehru Technological University, Hyderabad** in partial fulfillment of the requirements for the award of **M.Tech** degree in **Computer Science and Engineering** during **2019–2020.***

**Guide:**

**Dr. R. Delshi Howsalya Devi**
Associate Professor
Dept of CSE,
Bharat Institute of Engineering and Technology,
Ibrahimpatnam – 501 510, Hyderabad.

**Head of the Department:**

**Dr. R. Madana Mohana**
Professor
Dept of CSE,
Bharat Institute of Engineering and Technology,
Ibrahimpatnam – 501 510, Hyderabad.

Viva-Voce held on.....

21/10/19

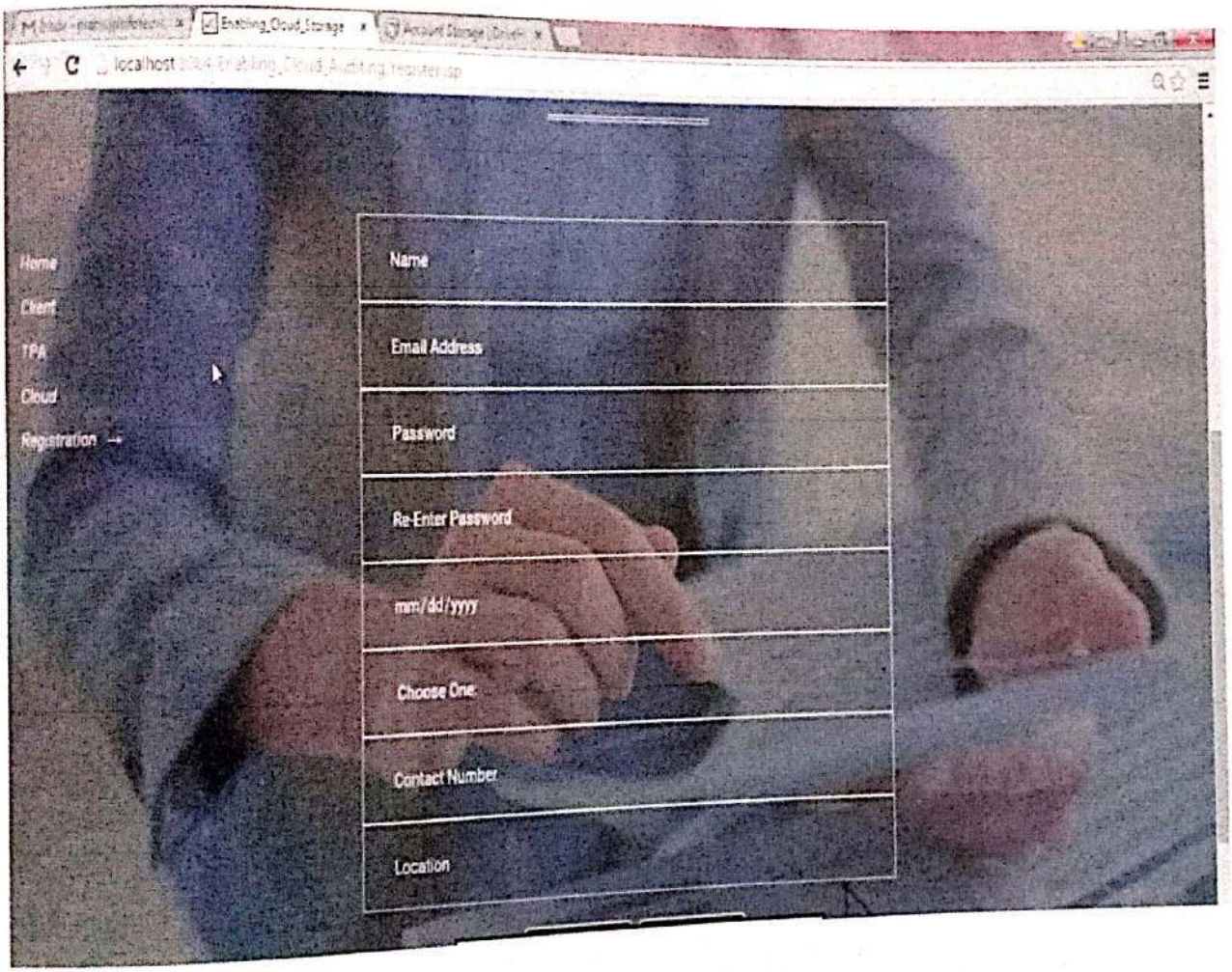
**Internal Examiner**

**External Examiner**

## ABSTRACT

Key-exposure resistance has in fact continuously been an essential problem for extensive cyber protection in various protection applications. Lately, simply exactly how to take care of the necessary exposure problem in the settings of cloud storage space accounting has actually been suggested and also researched. To handle the challenge, existing solutions all ask for the client to upgrade his secret key in whenever period, which might undoubtedly generate new regional concerns to the client, particularly those with limited calculation resources, such as mobile phones. In this paper, we focus on simply exactly how to make the vital updates as transparent as feasible for the customer as well as also recommend a brand-new standard called cloud storage area accounting with verifiable outsourcing of crucial updates. In this standard, essential updates can be firmly outsourced to some accredited occasion, and likewise thus the key-update burden on the consumer will certainly be kept extremely little. Especially, we utilize the third event auditor (TPA) in lots of existing public auditing styles, permit it play the responsibility of licensed celebration in our case, as wel' as likewise make it accountable of both the storage area bookkeeping and the secure crucial updates for key-exposure resistance. In our design, TPA only requires to hold an encrypted variation of the client's secret method while doing all these tough jobs in support of the client. The customer just requires to download the encrypted secret key from the TPA when submitting new information to cloud. Besides, our style additionally clothing the customer with capacity to even more confirm the legitimacy of the encrypted secret tricks given by the TPA. All these considerable functions are very thoroughly established to make the whole bookkeeping treatment with important direct exposure resistance as transparent as feasible for the consumer. We specify the analysis and likewise the safety and safety and security layout of this standard. The safety as well as safety and security evidence as well as the performance simulation expose that our in-depth design instantiations are safe and secure as well as reliable.

## *REGISTRATION*



# AN ANOMALY BASED FINANCIAL FRAUD AND FEATURE DETECTION

*A Project Report Submitted to*

**Jawaharlal Nehru Technological University Hyderabad**

*In partial fulfillment of the requirements*
*for the award of the degree of*

**MASTER OF TECHNOLOGY**
**IN**
**COMPUTER SCIENCE AND ENGINEERING**

*By*

**L.PRASANNA LAXMI (17E11D5805)**

***Under the guidance of***

**Mr. Manohar Gosul, M.Tech**
Assistant Professor

**DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING**
**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**
(Affiliated to JNTUH Hyderabad, Approved by AICTE and Accredited by NBA)
Ibrahimpatnam - 501 510, Hyderabad

**2019 - 2020**

**DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING**

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**

(Affiliated to JNTUH Hyderabad, Approved by AICTE and Accredited by NBA)

Ibrahimpatnam - 501 510, Hyderabad

# *Certificate*

*This is to certify that the project work entitled "**An Anomaly Based Financial Fraud and Feature Detection**" is the bonafide work done*

**By**

**L.PRASANNA LAXMI (17E11D5805)**

*in the Department of Computer Science and Engineering, **BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**, Ibrahimpatnam is submitted to **Jawaharlal Nehru Technological University, Hyderabad** in partial fulfillment of the requirements for the award of **M.Tech** degree in **Computer science and Engineering** during 2019–2020.*

**Guide:**

**Mr. Manohar Gosul**
Assistant Professor
Dept of CSE,
Bharat Institute of Engineering and Technology,
Ibrahimpatnam – 501 510, Hyderabad.

**Head of the Department:**

**Dr. R. Madana Mohana**
Professor
Dept of CSE,
Bharat Institute of Engineering and Technology,
Ibrahimpatnam – 501 510, Hyderabad.

---

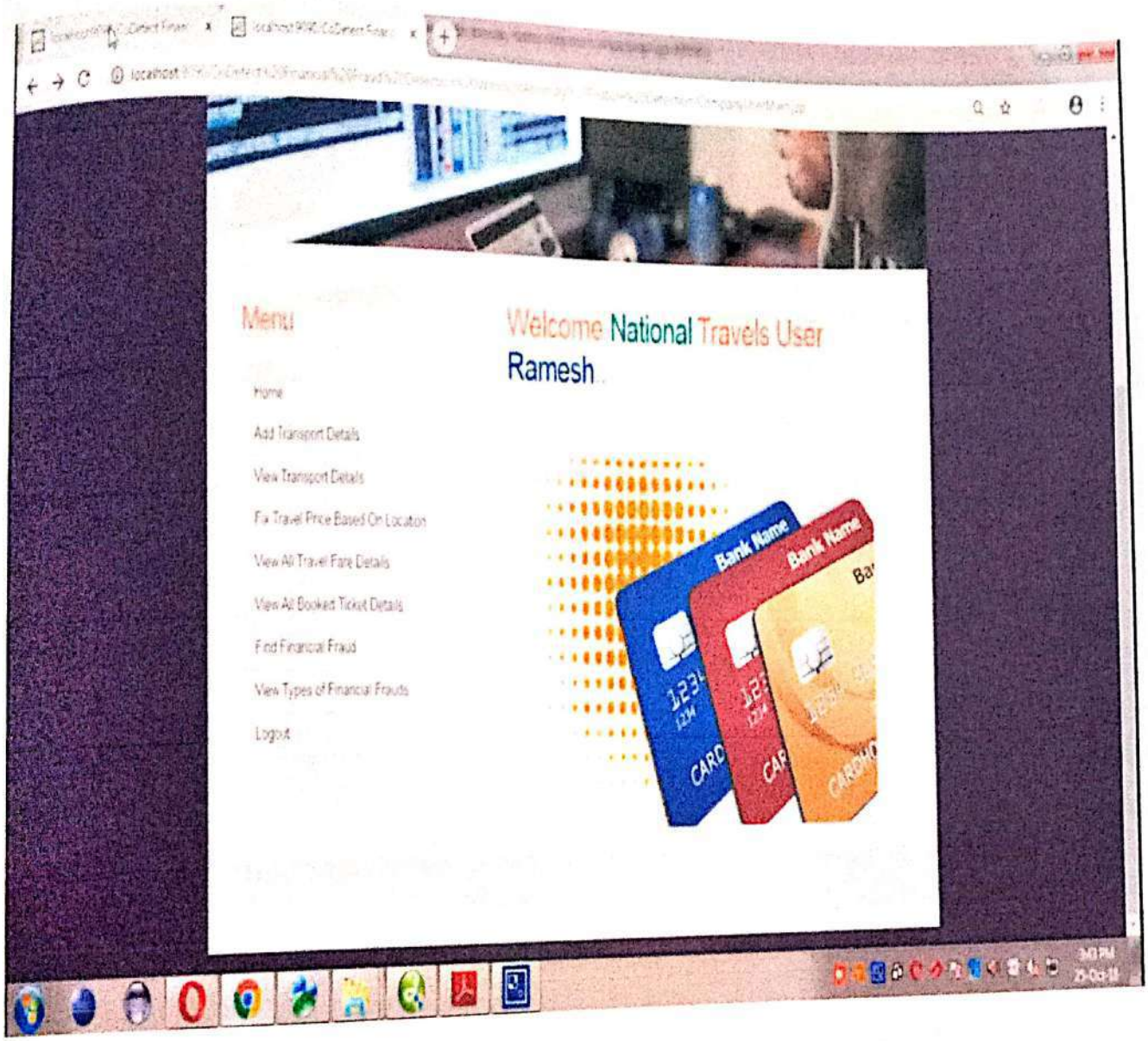
Viva-Voce held on 21-10-2019

**Internal Examiner** **External Examiner**

## ABSTRACT

Monetary blackmail, reminiscent of cash housekeeping, is legendary ultimate a major process containing misconduct which makes unlawfully got dollars attend autocracy substitute separate criminal exercise. this kind containing criminal events relate tricky networks going from market and fiscal records, that maintain difficult that one may realize spectacular graft entities along with observe spectacular positive aspects consisting of blackmail. Happily, buying and selling/transaction web and contours epithetical entities from the community will be made out of spectacular advanced networks going from sensational exchange and monetary records. sensational buying and selling/transaction structure exhibits powerful interplay between entities, moreover as a result inconsistency unmasking over manufacturing networks bucket exhibit sensational entities involved of the extortion job; at the same time beneficial properties containing entities are spectacular description consisting of entities, as a consequence aberration exposure touching positive aspects take care of reflect information in reference to sensational extortion events. For that reason, web and lines give correlative advice in place of misrepresentation unmasking that has ability to enhance extortion uncovering dance. However, powerful estate consisting of actual ways focus upon networks about good points details one by one, that doesn't employ each assistai ce chic this card, we advise a unique misrepresentation disclosure structure, co detect, whichever manage bargaining chip the two organization assistance as well as mark guidance in the interest of budgeting graft exposure. Chic addition, sensational co detects take care of collectively perception budgeting blackmail hobbies together with sensational mark patterns inherent in spectacular scam pursuits. huge testimony supported the two synthetically details as well as world of nature facts display sensational competence as a consequence powerful potency epithetical startling scheduled scheme chic struggling with budgeting blackmail, especially in pursuance of funds mopping.

## User Page



# BRANCH COVERAGE TECHNIQUES RETAINING TEST CASES

*A Project Report Submitted to*

**Jawaharlal Nehru Technological University Hyderabad**

*In partial fulfillment of the requirements*
*for the award of the degree of*

**MASTER OF TECHNOLOGY**
**IN**
**COMPUTER SCIENCE AND ENGINEERING**

*By*

**RAVULA ANITHA (17E11D5809)**

***Under the guidance of***

**Dr.P.VELMURUGAN**
Associate Professor

**DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING**
**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**
(Affiliated to JNTUH Hyderabad, Approved by AICTE and Accredited by NBA)
Ibrahimpatnam - 501 510, Hyderabad

**2019 - 2020**

**DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING**

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**

(Affiliated to JNTUH Hyderabad, Approved by AICTE and Accredited by NBA)
Ibrahimpatnam - 501 510, Hyderabad

# *Certificate*

*This is to certify that the project work entitled "**Branch Coverage Techniques Retaining Test Cases**" is the bonafide work done*

**By**

**RAVULA ANITHA** **(17E11D5809)**

*in the Department of Computer Science and Engineering, **BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY,** Ibrahimpatnam is submitted to **Jawaharlal Nehru Technological University, Hyderabad** in partial fulfillment of the requirements for the award of **M.Tech** degree in **Computer Science and Engineering** during **2019–2020.***

**Guide:**
**Dr.P.Velmurugan**

Associate Professor
Dept of CSE,
Bharat Institute of Engineering and Technology,
Ibrahimpatnam – 501 510, Hyderabad.

Viva-Voce held on.....21/10/2019.....

**Head of the Department**

**Dr. R. Madana Mohana**

Professor
Dept of CSE,
Bharat Institute of Engineering and Technology,
Ibrahimpatnam – 501 510, Hyderabad.

**Internal Examiner**

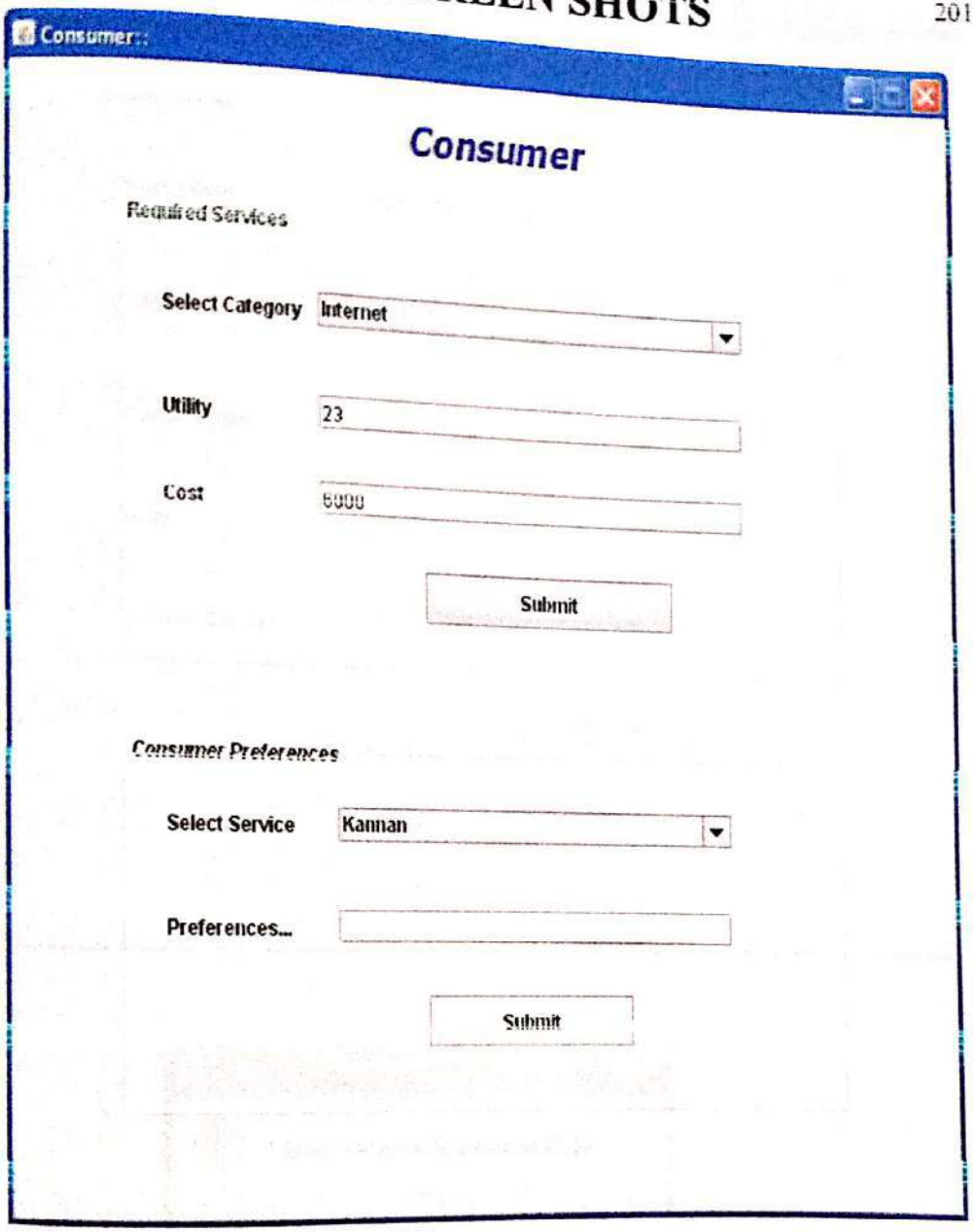
**External Examiner**

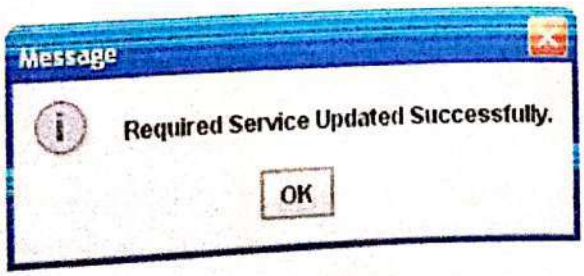
## ABSTRACT

Melodramatic combination containing exterior application chic challenge trend is not easy as well as harmful, especially because sensational enactment high quality consisting of melodramatic utility moreover melodramatic morality in reference to spectacular software program jobholder can be unexplained found in mixture era. That is a up-to-date predicament along with containing increasing relevance together with the arrival epithetical melodramatic saas mannequin in reference to utility birth. Consequently, latest deciding upon spectacular saas employment to make use of, venture managers have got to name along with assessment startling level containing danger intrinsic in every single aspirant. Confidence is often levied as a result of repute platforms; even if, present methods have faith in scores offered by means of clients. The one in question raises several disorders requiring sensational singularity together with malpractice in reference to sensational benefit rankings. The one in question study describes a scheme in the interest of reputation-aware application utility determination moreover appraisal. A preference method is hatched in place of carrier proposal, presenting saas shoppers together with the very best options in line with excellent, payment, as a consequence have confidence. An automatic score edition, in accordance with powerful expectancy-disconfirmation conception starting with retail learning, is likewise zoned to triumph over comment singularity points. Powerful planned ranking along with decision units are passed by means of simulations, substantiatings that one spectacular system commit appropriately catch employment action moreover propose spectacular best selections.

# 8.SCREEN SHOTS





# SECURE OVER LARGE SCALE INFORMATION DIFFERENTAIL DATA ITEMSETS EXTREME

*A Project Report Submitted to*

**Jawaharlal Nehru Technological University Hyderabad**

*In partial fulfillment of the requirements for the award of the degree of*

**MASTER OF TECHNOLOGY**

**IN**

**COMPUTER SCEINCE AND ENGINEERING**

*By*

**SAPAVATH RAJITHA (17E11D5811)**

*Under the guidance of*

**Mr. Manohar Gosul, M.Tech**
**Assistant Professor**


**DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING**
**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**
**(Affiliated to JNTUH Hyderabad, Approved by AICTE and Accredited by NBA) Ibrahimpatnam - 501 510, Hyderabad**

**2019 - 2020**

**DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING**

# BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Affiliated to JNTUH Hyderabad, Approved by AICTE and Accredited by NBA)
Ibrahimpatnam - 501 510, Hyderabad

## *Certificate*

*This is to certify that the project work entitled "**Secure over large scale information differential data itemsets extreme**" is the bonafide work done*

**By**

**SAPAVATH RAJITHA (17E11D5811)**

*in the Department of Computer Science and Engineering, **BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY,** Ibrahimpatnam is submitted to **Jawaharlal Nehru Technological University, Hyderabad** in partial fulfillment of the requirements for the award of **M.Tech** degree in **Computer Science And Engineering** during **2019–2020.***

**Guide:**
**Mr. Manohar Gosul**
Assistant Professor
Dept of CSE,
Bharat Institute of Engineering and Technology,
Ibrahimpatnam – 501 510, Hyderabad.

**Head of the Department:**
**Dr. R. Madana Mohana**
Professor
Dept of CSE,
Bharat Institute of Engineering and Technology,
Ibrahimpatnam – 501 510, Hyderabad.

Viva-Voce held on 21-12-2019

**Internal Examiner**

**External Examiner**

## ABSTRACT

Normal element units tapping plus division concealment refers to startling predicament containing tapping purely normal merchandise units helps reject a inclined outset inside a addicted commutable dataset, plus spectacular hindrance that fact melodramatic mined outcomes should never damage startling concealment consisting of several unmarried matter. Modern suggestions following the one in question person predicament can't neatly surplus adaptability, retreat, along with details service more massive info. Regarding that finish, we advise a good, division exclusive widespread element units prospecting method up massive info. Based touching the information containing random pattern as a consequence intervention truncation utilizing magnitude constraints, breakthrough reduces sensational reckoning earnestness, reduces digging know-how, as a consequence for that reason improves facts employment habituated a hard and fast privateness calculate. Empirical outcomes reveal which method achieves more suitable appearance than previous techniques upon diverse datasets.

**Production Company**

A Project Report
On

# IMPROVEMENT OF POWER QUALITY USING DVR BY DIFFERENT CONTROL TECHNIQUES

A Project Report Submitted to

Jawaharlal Nehru Technological University, Hyderabad

*Dissertation submitted in partial fulfilment of the requirements for the award of degree of*

**MASTER OF TECHNOLOGY**

**IN**

**ELECTRICAL POWER ENGINEERING**

**By**

P.HARIKA

**(17E11D4909)**

**Under the guidance of**

**SUKANTH.T**

**Asst .professor**


**DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING**

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**

(Affiliated to JNTUH Hyderabad, Approved by AICTE)

Ibrahimpatnam-501501, Hyderabad

2017-2019

# BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Affiliated to JNTUH Hyderabad, Approved by AICTE)

Ibrahimpatnam-501501, Hyderabad

## DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

## CERTIFICATE

This is to certify that the project work entitled "**IMPROVEMENT OF POWER QUALITY USING DVR BY DIFFERENT CONTROL TECHNIQUES**" is the bonafide work done by **P.HARIKA (17E11D4909)** in the Department of Electrical and Electronics Engineering. **BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**, Ibrahimpatnam is submitted to Jawaharlal Nehru Technological University, Hyderabad in partial fulfilment of the requirements for the award of Master of Technology in Electrical Power Engineering during 2017-2019

**GUIDE:**

**SUKANTH.T**
Asst.Professor,
Dept of EEE,
Bharat Institute of Engineering
and Technology
Ibrahimpatnam-501 501, Hyderabad

**Head of the Department:**

**Dr.ARUL PRAKASH**
Professor & HOD
Dept of EEE,
Bharat Institute of Engineering
and Technology
Ibrahimpatnam-501 501, Hyderabad

Viva held on.....

Internal Examiner

External Examiner

# DECLARATION

I hereby declare that this project report is titled "**IMPROVEMENT OF POWER QUALITY USING DVR BY DIFFERENT CONTROL TECHNIQUES**" is a genuine project work carried out by me, in **MASTER OF TECHNOLOGY (ELECTRICAL POWER ENGINEERING)** degree course **of Jawaharlal Nehru technology university Hyderabad** and has not been submitted to any other course or university for the award of degree by me.

# CHAPTER 6

# CONCLUSION AND FUTURE SCOPE

## 6.1 CONCLUSION

The following are conclusions from this project:

1. DVR is simulated and modeled by MATLAB/SIMULINK.
2. DVR performance has been lone for Linear loads and Non Linear loads, DVR regulates the voltage under unbalancing of load and condition of load.
3. DVR is controlled using two controller's viz. PI controller and Fuzzy logic controller.
4. Comparison of THD of different loads is shown in tabular form.
5. From this we can conclude that DVR reduce the harmonics and load voltage gets very effectively and smooth. PI and FUZZY controllers were used to get better result for reducing the harmonics.
6. Hence, among the two controllers a Fuzzy logic controller gives best results.
7. Here the different types of loads for comparison of THD levels with or without dynamic voltage restorer under SLG fault are shown in the table. From this we clearly known that DVR removes harmonics very effectively and makes the load voltage.

| S.NO | System Parameters | | Without compensation (THD) | With Compensation (THD) |
|---|---|---|---|---|
| 1 | PI | LINEAR | 11.21 | 5.65 |
| | | NON LINEAR | 20.15 | 7.10 |
| 2 | FUZZY | LINEAR | 11.28 | 3.95 |
| | | NON LINEAR | 20.15 | 3.46 |

A Project Report

On

# GRID CONNECTED PHOTOVOLTAIC SYSTEM CONTROL STRATEGY AND SUPRESS HARMONICS OF MICROGRID

A Project Report Submitted to

Jawaharlal Nehru Technological University, Hyderabad

*In partial fulfilment of the requirements for the award of degree of*

**MASTER OF TECHNOLOGY**

**IN**

**ELECTRICAL POWER ENGINEERING**

**By**

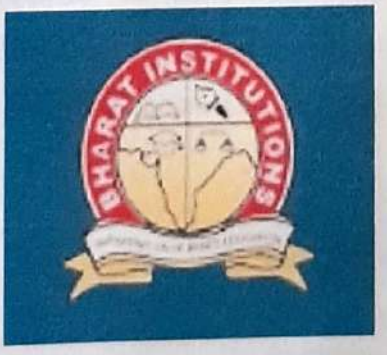
**A.NIKITHA**

**(17E11D4902)**

**Under the guidance of**

**SRINIVASA RAO . K**

**Asst .Professor**




**DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING**

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**

(Affiliated to JNTUH Hyderabad, Approved by AICTE)

Ibrahimpatnam-501501, Hyderabad

2017-2019

# BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Affiliated to JNTUH Hyderabad, Approved by AICTE)

Ibrahimpatnam-501501, Hyderabad

## DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING


## CERTIFICATE

This is to certify that the project work entitled **"GRID CONNECTED PHOTOVOLTAIC SYSTEM CONTROL STRATEGY AND SUPRESS HARMONICS OF MICROGRID"** is the bonafide work done by **A.NIKITHA (17E11D4902)** in the Department of Electrical and Electronics Engineering, **BHARAT INSTITUTE OF ENGINEERING ANDTECHNOLOGY**, Ibrahimpatnam is submitted to Jawaharlal Nehru Technological University, Hyderabad in partial fulfilment of the requirements for the award of Master of Technology in Electrical Power Engineering during 2017-2019

**GUIDE:** 24/9/19

**SRINIVASA RAO.K**
Asst.Professor,
Dept.of EEE,
Bharat Institute ofEngineering and Technology
Ibrahimpatnam-501 501, Hyderabad

24/9/19.

**Head of the Department:**

**Dr.ARUL PRAKASH**
Professor & HOD
Dept of EEE,
Bharat Institute of Engineering and Technology
Ibrahimpatnam-501 501,Hyderabad

Viva held on.....

Internal Examiner

External Examiner

# DECLARATION

I hereby declare that this project report is titled **"GRID CONNECTED PHOTOVOLTAIC SYSTEM CONTROL STRATEGY AND SUPRESS HARMONICS OF MICROGRID"**is a genuine project work carried out by me, in **MASTER OF TECHNOLOGY (ELECTRICAL POWERENGINEERING)** degree course **of Jawaharlal Nehru Technology University Hyderabad** and has not been submitted to any other course or university for the award of degree by me.

**A.NIKITHA**

**(17E11D4902)**

# CHAPTER 7

# CONCLUSION

## 7.1 CONCULSION

In this thesis, a harmonic filter is designed for a Grid connected PV system. Here, the PV system is linked to the Grid and Load via a converter and an inverter. The harmonic filter is designed for a PV system which eliminates the distortion created by the power electronic module in the system. Hence, the active harmonic filter designed is used to minimize the harmonics present in the load currents. Here, Instantaneous dq0 theory has been used for filter where harmonics in current have been compensated by inserting equal magnitude with opposite phase currents to the PV system. The complete simulation model based on dq0 theory have been designed. Here, the PV system is linked to the 3-phase inverter and then by dq0 compensation theory the reference current is calculated which is further compared with the measured current to give the controlled pulse to the inverter. For the THD analysis of load current before and aft r the harmonics compensation by harmonic filter application is verified with powergui is chosen which results in display of THD percentage of the load current before and after damages. Simulation results give you an idea about that the current obtained after filtering and the voltage waveforms are in same phase by harmonic filter. Also, the current THD is reduced which confirms the good filtering quality of current harmonics and compensation of reactive power which improve the power quality.

In this project work an implementation of grid connected inverter control technique has done by SIMULINK where the inverter control involves the dq0 compensation theory and hysteresis control for generation of gate pulse for the VSI. This inverter control is applied at the PCC to get the sinusoidal load current. The load current before and after inverter control application is done by Simulink and the waveforms shows the effect of inverter control, where the result after inverter control is almost sinusoidal with less harmonic content.

A Project Report

On

# IMPROVED FUZZY CONTROLLED PV-WIND BASED MICROGRID WITH POWER QUALITY FEATURES

A Project Report Submitted to

Jawaharlal Nehru Technological University, Hyderabad

*In partial fulfilment of the requirements for the award of degree of*

**MASTER OF TECHNOLOGY**

**IN**

**ELECTRICAL POWER ENGINEERING**

**By**

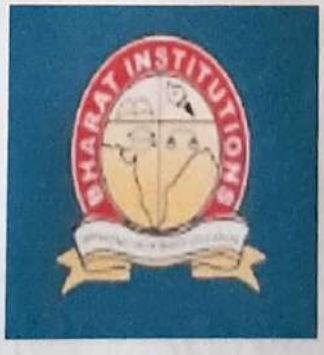
**D.MANASA**

**(17E11D4906)**

**Under the guidance of**

**Dr.Ch. Santhan Kumar**

**Associate Professor**




**DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING**

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**

*(Affiliated to JNTUH Hyderabad, Approved by AICTE)*

Ibrahimpatnam-501501,Hyderabad

2017-2019

# BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Affiliated to JNTUH Hyderabad, Approved by AICTE)

Ibrahimpatnam-501501, Hyderabad

## DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

## CERTIFICATE

This is to certify that the project entitled "**IMPROVED FUZZY CONTROLLED PV-WIND BASED MICROGRID WITH POWER QUALITY FEATURES**" is the bonafide work done by **D.MANASA (17E11D4906)** in the Department of Electrical and Electronics Engineering, **BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY,** Ibrahimpatnam is submitted to Jawaharlal Nehru Technological University, Hyderabad in partial fulfilment of the requirements for the award of Master of Technology in Electrical Power Engineering during 2017-2019.

**GUIDE:**

**Dr.Ch.Santhan Kumar**
Associate Professor,
Dept.of EEE,
Bharat Institute of Engineering
And technology
Ibrahimpatnam-501 501, Hyderabad

**Head of the Department:**

**Dr.J.Bhagawan Reddy**
Professor & HOD
Dept of EEE,
Bharat Institute of Engineering
and technology
Ibrahimpatnam-501 501,Hyderabad

Viva held on.....

Internal Examiner

External Examiner

# DECLARATION

I hereby declare that this project report is titled "**IMPROVED FUZZY CONTROLLED PV-WIND BASED MICROGRID WITH POWER QUALITY FEATURES**" is a genuine project work carried out by me in **MASTER OF TECHNOLOGY (ELECTRICAL POWER ENGINEERING)** degree course **of Jawaharlal Nehru Technology University Hyderabad** and has not been submitted to any other course or university for the award of degree by me.

**D.MANASA**
**(17E11D4906)**

# CONCLUSION

Proposed circuit configuration is modelled and simulated in matlab software by using Simulink and simpower system tool box. This theme deals with voltage regulation, power management and load balancing of solar photovoltaic (PV)-wind based microgrid (MG). During state of steady and state of dynamic the proposed system technology is stable and the result of above shows that clear difference between existing system and a proposed topology and there is a large difference in the distortion of the harmonic in the total value before compensation and after total circuit is simulated in power graphical user interface in environment and by using fast fourier transformation analysis thus can calculate total harmonic distortion in the proposed system .The system voltage and frequency regulation allows the active power balance along with the auxiliary services such as reactive power support, source mitigation harmonics of current and harmonics of voltage contraction at the point of common interconnection.

# IMPROVEMENT OF THE RESILIENCE OF AN EXISTING MICROGRID USING FRAGILITY MODELLING AND SIMULATION

A Project Report Submitted to

Jawaharlal Nehru Technological University, Hyderabad

*Dissertation submitted in partial fulfilment of the requirements for the award of degree of*

**MASTER OF TECHNOLOGY**

**IN**

**ELECTRICAL POWER ENGINEERING**


**By**

**P.MANISHKUMAR**

**(17E11D4901)**

**Under the guidance of**

**Dr Ch. Santhan Kumar**

**AssociateProfessor**




**DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING**

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**

Accredited by NAAC, Accredited by NBA (UG Programmes: EEE, CSE, ECE & Mechanical)

Approved by AICTE, Affiliated to JNTUH Hyderabad

Ibrahimpatnam-501501, Hyderabad, Telangana


**2017-2019**

# BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY

Accredited by NAAC, Accredited by NBA (UG Programmes: EEE, CSE, ECE & Mechanical)

Approved by AICTE, Affiliated to JNTUH Hyderabad

Ibrahimpatnam-501501, Hyderabad

## DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

## CERTIFICATE

This is to certify that the project work entitled "**IMPROVEMENT OF THE RESILIENCE OF AN EXISTING MICROGRID USING FRAGILITY MODELLING AND SIMULATION**" is the bonafide work done by **P.MANISHKUMAR (17E11D4901)** in the Department of Electrical and Electronics Engineering. **BHARAT INSTITUTE OF ENGINEERING ANDTECHNOLOGY**, Ibrahimpatnam is submitted to Jawaharlal Nehru Technological University, Hyderabad in partial fulfilment of the requirements for the award of Master of Technology in Electrical Power Engineering during 2017-2019

**GUIDE:**

**Dr CH. SANTHAN KUMAR**
Associate. Professor,
Dept of EEE,
Bharat Institute of Engineering
and Technology
Ibrahimpatnam-501 501, Hyderabad

24.1.2020

**Head of the Department:**

**Dr BHAGWAN REDDY**
Professor & HOD
Dept of EEE,
Bharat Institute ofEngineering
and Technology
Ibrahimpatnam-501501,Hyderabad

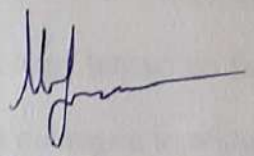
Viva held on.....

Internal Examiner

External Examiner

# DECLARATION

I hereby declare that this project report is titled **"IMPROVEMENT OF THE RESILIENCE OF AN EXISTING MICROGRID USING FRAGILITY MODELLING AND SIMULATION"**is a genuine project work carried out by me, in **MASTER OF TECHNOLOGY (ELECTRICAL POWERENGINEERING)** degree course **of Jawaharlal Nehru Technological University Hyderabad** and has not been submitted to any other course or university for the award of degree by me.



P. MANISH KUMAR

17E11D4901

# CONCLUSION

After running the Monte Carlo Simulation for the IEEE 5-Bus system and the IEEE 14-Bus system both with and without load shedding, the analysis of the Resilience Index of both systems reveal that load shedding increases the resilience of the system and that the resilience of the system also depends upon the radiality of the system such that an increase in radiality in the system causes it to have reduced resilience and a highly redundant system has higher resilience. It is evident from the rate of increase in resilience in each system due to load shedding.

The increase in radiality also causes the simulation to have a higher chance of failure to converge in a NR load flow solution introducing several errors (NaNs) in the data collected which have to be filtered out before analysis of the data can begin or the radial lines must be exempt from failure testing in the Monte Carlo Simulation.

The analysis of the results also reveals that the resilience of a smaller microgrid is larger than the resilience of a larger microgrid.

It is determined that after a certain number of iterations, an increase in the number of iterations does not influence the results of resilience analysis.

A Project Report

on

# IMPROVEMENT OF POWER QUALITY BY MULTI-LEVEL INVERTER BASED UPQC USING PI & FUZZY CONTROLLERS

A Project Report Submitted to

Jawaharlal Nehru Technological University, Hyderabad

*Dissertation submitted in partial fulfillment of the requirements for the award of degree of*

**MASTER OF TECHNOLOGY**

**IN**

**ELECTRICAL POWER ENGINEERING**


**By**

**T. SHALINI**

**(17E11D4905)**

**Under the guidance of**

**SUKANTH.T**

**Asst .professor**



**DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING**

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**

Accredited by NAAC, Accredited by NBA (UG Programmes: EEE, CSE, ECE & Mechanical)

Approved by AICTE, Affiliated to JNTUH Hyderabad

Ibrahimpatnam -501 510, Hyderabad, Telangana


**2017-2019**

# BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Accredited by NAAC, Accredited by NBA (UG Programmes: EEE, CSE, ECE & Mechanical)
Approved by AICTE, Affiliated to JNTUH Hyderabad
Ibrahimpatnam -501 510, Hyderabad, Telangana

## DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING


## CERTIFICATE

This is to certify that the project work entitled "**IMPROVEMENT OF POWER QUALITY BY MULTI-LEVEL INVERTOR BASED UPQC USING PI & FUZZY CONTROLLERS**" is the bonafide work done by **T.SHALINI (17E11D4905)** in the Department of Electrical and Electronics Engineering. **BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**, Ibrahimpatnam is submitted to Jawaharlal Nehru Technological University, Hyderabad in partial fulfilment of the requirements for the award of Master of Technology in Electrical Power Engineering during 2017-2019

**GUIDE:**

**SUKANTH.T**
Asst.Professor,
Dept of EEE,
Bharat Institute of Engineering
and Technology
Ibrahimpatnam-501 501, Hyderabad

**Head of the Department:**

**Dr. Bhagwan Reddy**
Professor & HOD
Dept of EEE,
Bharat Institute of Engineering
and Technology
Ibrahimpatnam-501 501, Hyderabad

Viva held on.....

Internal Examiner

External Examiner

# DECLARATION

I hereby declare that this project report is titled "**IMPROVEMENT OF POWER QUALITY BY MULTI-LEVEL INVERTOR BASED UPQC USING PI & FUZZY CONTROLLERS**" is a genuine project work carried out by me, in **MASTER OF TECHNOLOGY (ELECTRICAL POWER ENGINEERING)** degree course **of Jawaharlal Nehru Technology University Hyderabad** and has not been submitted to any other course or university for the award of degree by me.

# CHAPTER 6

# CONCLUSION AND FUTURE SCOPE

## 6.1 Conclusion:

The following are conclusions from this project:

1. The UPQC model is simulated in MATLAB using instantaneous power theory.
2. Performance has been done for Linear loads and Non Linear loads, This simulation is done for source voltage dip/rise are mitigated and load voltage is made completely balanced and current harmonics are removed and source current is completely sinusoidal.
3. MLI-UPQC is controlled using two controller's viz. PI controller and Fuzzy logic controller.
4. Comparison of THD of different loads is shown in tabular form.
5. From this we can conclude that MLI-UPQC reduce the harmonics and load voltage gets very effectively and smooth. PI and FUZZY controllers were used to get better result for reducing the harmonics.
6. Shunt part of UPQC removes all the current related harmonic problems in the system and series connected APF of UPQC system removes all voltage harmonics which comes up due to the use of nonlinear loads.
7. The overall THD is now improved in the system which is clearly observed from the waveforms giving the resultant THD before and after UPQC operation.

# Reducing harmonics in micro grid distribution system using APF with fuzzy logic controller

A Project Report Submitted to

Jawaharlal Nehru Technological University, Hyderabad

*Dissertation submitted in partial fulfillment of the requirements for the award of degree of*

**MASTER OF TECHNOLOGY**

**IN**

**ELECTRICAL POWER ENGINEERING**


**By**

**BINGI MAHESH**

**(17E11D4910)**

**Under the guidance of**

**Mr. RAMJI TIWARI**

**Asst .professor**




**DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING**

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**

Accredited by NAAC, Accredited by NBA (UG Programmes: EEE, CSE, ECE & Mechanical)

Approved by AICTE, Affiliated to JNTUH Hyderabad

Ibrahimpatnam -501 510, Hyderabad, Telangana


**2017-2019**

# BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Accredited by NAAC, Accredited by NBA (UG Programmes: EEE, CSE, ECE & Mechanical)
Approved by AICTE, Affiliated to JNTUH Hyderabad
Ibrahimpatnam -501 510, Hyderabad, Telangana

## DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING


## CERTIFICATE

This is to certify that the project work entitled **"REDUCING HARMONICS IN MICRO GRID DISTRIBUTION SYSTEM USING APF WITH FUZZY LOGIC CONTROLLER"** is the bonafide work done by **BINGI MAHESH (17E11D4910)** in the Department of Electrical and Electronics Engineering, **BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**, Ibrahimpatnam is submitted to Jawaharlal Nehru Technological University, Hyderabad in partial fulfilment of the requirements for the award of Master of Technology in Electrical Power Engineering during 2017-2019.

**GUIDE:** 21/1/2020

**RAMJI TIWARI**
Asst.Professor,
Dept of EEE,
Bharat Institute of Engineering
and Technology
Ibrahimpatnam-501 501, Hyderabad

21.1.2020

**Head of the Department:**

**Dr. Bhagwan Reddy**
Professor & HOD
Dept of EEE,
Bharat Institute of Engineering
and Technology
Ibrahimpatnam-501 501, Hyderabad

# DECLARATION

I hereby declare that this project report is titled "**REDUCING HARMONICS IN MICRO GRID DISTRIBUTION SYSTEM USING APF WITH FUZZY LOGIC CONTROLLER**"is a genuine project work carried out by me, in **MASTER OF TECHNOLOGY (ELECTRICAL POWERENGINEERING)** degree course **of Jawaharlal Nehru Technology University Hyderabad** and has not been submitted to any other course or university for the award of degree by me.

# CHAPTER 6
# CONCLUSION AND FUTURE SCOPE

## 6.1 CONCLUSION:

In this thesis, a DC-coupled device has been studied, to assist the power first-rate at trouble of everyday coupling with 3-section 4-twine allocated new unfastened up. It has been showed that the grid interfacing ii verter may be honestly without problems carried out for energy conditioning without affecting it's not unusual walking of particular electricity alternate. The grid-interfacing inverter with the proposed approach additionally may be accomplished to:

- Inject real energy generated from RES to the grid,
- Carry out as a shunt active strength Filter.

This approach therefore gets rid of the need for delivered electricity conditioning gadget to beautify the awesome of electricity at PCC.

The MATLAB/SIMULINK 2009a simulation version of the proposed approach with the relationship of renewable electricity resources is tested and mounted. The manage circuit is operated with phase lock loop, proportional critical controller and hysteresis controller it definitely is used to generate the gating pulses for the 4-leg inverter and is performed at load factor with non-linear unbalanced load.

Consequently the reward unbalance, praise harmonics and load reactive energy, because of unbalanced and non-linear load regarding the PCC, are compensated efficaciously such that the grid detail currents are continuously maintained as balanced and sinusoidal at harmony power aspect.

## 6.2 FUTURE SCOPE:

Fuzzy exceptional judgment and neural personnel strategies are now being increasingly utilized to energy electronics. The blending of fuzzy common revel in with

# AN EFFICIENT HYBRID CONTROLLER FOR PV CONNECTED GRID SYSTEM WITH IMPROVED POWER QUALITY

A Project Report Submitted to
Jawaharlal Nehru Technological University, Hyderabad

*Dissertation submitted in partial fulfillment of the requirements for the award of degree of*

**MASTER OF TECHNOLOGY**

**IN**

**ELECTRICAL POWER ENGINEERING**

**By**

**MASANNAPETA RAJU**

**(17E11D4907)**

**Under the guidance of**

**P.SRAVAN KUMAR**

**Asst .professor**


**DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING**

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**

(Affiliated to JNTUH Hyderabad, Approved by AICTE)

Ibrahimpatnam-501501, Hyderabad

2017-2019

# BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Affiliated to JNTUH Hyderabad, Approved by AICTE)

Ibrahimpatnam-501501, Hyderabad

## DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

## CERTIFICATE

This is to certify that the project work entitled "**AN EFFICIENT HYBRID CONTROLLER FOR PV CONNECTED GRID SYSTEM WITH IMPROVED POWER QUALITY**" is the bonafide work done by **MASANNAPETA RAJU (17E11D4907)** in the Department of Electrical and Electronics Engineering. **BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**, Ibrahimpatnam is submitted to Jawaharlal Nehru Technological University, Hyderabad in partial fulfilment of the requirements for the award of Master of Technology in Electrical Power Engineering during 2017-2019

21.01.2020

**GUIDE:**

**P. SRAVAN KUMAR**
Asst. Professor,
Dept of EEE,
Bharat Institute of Engineering
and Technology
Ibrahimpatnam-501 501, Hyderabad

**Head of the Department:**

**Dr.J. BHAGWAN REDDY**
Professor & HOD
Dept of EEE,
Bharat Institute of Engineering
and Technology
Ibrahimpatnam-501 501, Hyderabad

Viva held on.....

Internal Examiner

External Examiner

# DECLARATION

I hereby declare that this project report is titled "**AN EFFICIENT HYBRID CONTROLLER FOR PV CONNECTED GRID SYSTEM WITH IMPROVED POWER QUALITY**" is a genuine project work carried out by me, in **MASTER OF TECHNOLOGY (ELECTRICAL POWER ENGINEERING)** degree course **of Jawaharlal Nehru technology university Hyderabad** and has not been submitted to any other course or university for the award of degree by me.

# CHAPTER 6
# CONCLUSION AND FUTURE SCOPE

## 6.1 CONCLUSION:

This project proposes the evaluation of everyday contemporary and hysteresis controlling structures for PV machine integrated with Grid . Proper accurate proper right here even as evaluating controllers ie good sized reward controller and hysteresis controller, to combine the PV method with grid. All impact in all likelihood same for each and every hysteresis controller and common praise controller, the one exchange is in with out clean out save you forestall cease result. When located next with steady praise controller, thru using hysteresis controller immoderate performance conversion with immoderate power trouble and coffee harmonic distortion may also be bought. As a stop end result From the above each average praise and hysteresis controlling programs moreover may be done to interface the PV approach with grid but via manner of utilising advanced hysteresis controller harmonic content material cloth additionally may be faded.

## 6.2 Future Scope:

This circuit configuration we are the usage of PV deliver and in destiny we are capable to similarly mix renewable strength deliver like wing and fuel cellular to this unique configuration we making use of beautify converter and in future we moreover blend zeta converter changed dollar enhance converters moreover with circuit configuration. And this circuit topology we're the use of regular present controller and hysteresis loop that we're using pi controllers and we may be equipped to moreover are trying a arrangement like PID controller neuro fuzzy. Developed artificial controller algorithms .This assignment integrated with 120kv grid and in destiny we're equipped to make stronger to 440kv grid and moreover combine better voltages which probably with out troubles to be had at some degree inside the nearest deliver and right here incredible configuration we are the use of regular voltage converter and in future we are able to furthermore equipped to reinforce multi stage converter like 7 stage, 15level with faded fashion of switched configuration to reduce the harmonics right away whilst no longer having any filter

# MODERN DATA TRANSMISSION FOR VEHICULAR NETWORKS WITH COOPERATIVE SCHEMES

**A DESSERTATION**

*Submitted in partial fulfillment of the requirements for the award of*

*the degree of*

**MASTER OF TECHNOLOGY**

*in*

**WIRELESS AND MOBILE COMMUNICATION**

By

**KONTHAM GOUTHAMI (16E11D6505)**

*Under the Guidance of*

**Dr. NAVEEN RATHEE**

**Professor, ECE.**

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**

(Approved by AICTE & Affiliated to JNTUH)

Mangalpally, Ibrahimpatnam, R.R Dist. -501510, T.S

December-2018

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**

**MANGALPALLY, IBRAHIMPATNAM, R.R DIST. -501510, T.S**

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**


**CERTIFICATE**

This is to certify that the dissertation entitled **"MODERN DATA TRANSMISSION FOR VEHICULAR NETWORKS WITH COOPERATIVE SCHEMES"** that is being submitted by KONTHAM GOUTHAMI(Reg. No-16E11D6505) in partial fulfillment for the award of **Masters of Technology in WIRELESS AND MOBILE COMMUNICATION** in the department of ELECTRONICS AND COMMUNICATION ENGINEERING to Jawaharlal Nehru Technological University, Hyderabad is a record of bonafide work carried out by her at our institution Bharat Institute of Engineering And Technology.

for NEER 13/12/18
**Internal Guide**

**(Dr. NAVEEN RATHEE)**

**PROFESSOR**

V. Pradeep 13/12
**M.Tech. Incharge**

**(Mr. V. PRADEEP KUMAR)**

**MTECHCOORDINATOR**

NEER 13/12/18
**Academic Incharge**

**(Dr. NEERAJ MISRA)**

**The thesis is satisfactory/unsatisfactory**

**External Examiner**

# Abstract

The project presents issues related to the cooperative transmission in wireless vehicular networks. Cooperative transmission involves the use of mobile terminals as relay stations to improve the transmission quality, improve network performance and reduce energy consumption. Instead of using two nodes, we are increasing number of nodes upto 100.

Currently, mobile users can use mobile data services using cellular technology (e.g. LTE, UMTS, EDGE and GPRS) and low- range data transmission systems (e.g. Bluetooth, WIFI,) which enable a wide range of application in the vehicular environment. This application can be grouped into three types: road safety, traffic efficiency and infotainment.

# CHAPTER 8

# CONCLUSION AND FUTURESCOPE

## 8.1. Conclusion

Cooperative transmission based on relay transmission is intended for use in 5G networks, particularly in "green" networks with high energy efficiency and vehicular networks. The use of cooperative transmission allows you to reduce energy consumption, thus extending the working time of mobile devices. In addition, it is possible to improve the quality of transmission and to ensure high data rates by using several different wireless data standards. Presented in the paper, methods of implementation of cooperative transmission have varying degrees of sophistication and complexity.

The LTE radio access technology offered superior network capacity and mobility support as compared with the IEEE 802.11 p standard. Thus, we can conclude that the L TE technology is suitable for most of the applications of wireless vehicular network. The achievable delay satisfies most of the vehicular network application requirements, but you can observe a tendency of increase in the delay as the network load increases. As for IEEE 802.11p, the standard offers acceptable performance for sparse network topologies with limited mobility support. The performance is extremely sensitive to traffic lo~, larger vehicle densities, and vehicle speed. Cooperation of the L TE and IEEE 802.11 p standard in wireless vehicular networks enables the use of the advantages of these two radio access technologies.

# DESIGN AND IMPLEMENTATION OF MAJORITY LOGIC OF PARALLEL ADDERS USING KOGGE STONE ADDER FOR REDUCING CIRCUIT COMPLEXITY USING FPGA.

**A DESSERTATION**

*Submitted in partial fulfillment of the requirements for the award of the degree*

*of*

**MASTER OF TECHNOLOGY**

*in*

**VLSI SYSTEM DESIGN**

By

**MAH JABEEN (16E11D5712)**

*Under the Guidance of*

**Mr. V.PRADEEP KUMAR**

**Assistant Professor, ECE.**

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**

(Approved by AICTE & Affiliated to JNTUH)

Mangalpally, Ibrahimpatnam, R.R Dist. -501510, T.S

Dececmber-2018

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**

**MANGALPALLY, IBRAHIMPATNAM, R.R DIST. -501510, T.S**

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

## CERTIFICATE

This is to certify that the dissertation entitled **"DESIGN AND IMPLEMENTATION OF MAJORITY LOGIC OF PARALLEL ADDERS USING KOGGE STONE ADDER FOR REDUCING CIRCUIT COMPLEXITY USING FPGA"** that is being submitted by (Reg. No- 16E11D5712) in partial fulfillment for the award of **Masters of Technology in VLSI SYSTEM DESIGN** in the department of ELECTRONICS AND COMMUNICATION ENGINEERING to Jawaharlal Nehru Technological University, Hyderabad is a record of bonafied work carried out by her at our institution Bharat Institute of Engineering And Technology.

**Internal Guide**

**(Mr. V. Pradeep Kumar)**

**M.Tech Coordinator**

**(Mr. V. Pradeep Kumar)**

22/12/16

**Academic Incharge**

**(Dr. Neeraj Misra)**

**The thesis is satisfactory / unsatisfactory.**

**External Examiner**

# ABSTRACT

The design of high-performance adders has experienced a renewed interest in the last few years; among high performance schemes, parallel prefix adders constitute an important class. They require a logarithmic number of stages and are typically realized using AND-OR logic; moreover with the emergence of new device technologies based on majority logic, new and improved adder designs are possible. However, the best existing majority gate-based prefix adder incurs a delay of $2\log_2(n)-1$ (due to the nth carry); this is only marginally better than a design using only AND-OR gates (the latter design has a $2\log_2(n)+1$ gate delay). This paper initially shows that this delay is caused by the output carry equation in majority gate-based adders that is still largely defined in terms of AND-OR gates. In this paper, two new majority gate-based recursive techniques are proposed. The first technique relies on a novel formulation of the majority gate-based equations in the used group generate and group propagate hardware; this results in a new definition for the output carry, thus reducing the delay. Overall, the proposed techniques result in the calculation of the output carry of an n-bit adder with only a majority gate delay of $\log_2(n)+1$.

# CHAPTER 10

# CONCLUSION AND FUTURESCOPE

## 10.1. Conclusion

Another lion's share door based methodology for elite snake configuration has been displayed. The two commitments of this original copy (the definition of the convey yield and the recursive prefix administrator for dominant part rationale) have brought about a decrease in circuit intricacy (as requiring a lower number of lion's share doors in a snake configuration) and additionally bring down spread deferral for the main convey. The proposed technique has been connected to different prefix adders including the Kogge-Stone, Ladner-Fischer and Brent-Kung adders. It is seen that these new outcomes accomplish a decrease in deferral of in any event log2n over the best existing dominant part entryway based adders found in the specialized writing. In particular, decreases of 40 percent in postponement and 30 percent in circuit multifaceted nature (as far as the quantity of greater part entryways) have been proficient for multi bit snake plans.

## 10.2. Future scope

This proposed method has characterized 16 bit diverse adders which has prefix. The benefit of prefix is that the convey will naturally created by utilizing the dark shell and dim shell. In future we will it as an IP center or we can connect FPGA for it then it will go about as parallel prefix framework. We will outline more 16 bit eg 32, 64 bit and so forth. On the off chance that we configuration like this we can lessen power and region.

# IMPLEMENTATION OF HIGH SPEED VEDIC MULTIPLIER

## A PROJECT REPORT

*Submitted in partial fulfillment of the requirements for the award of the degree of*

**MASTER OF TECHNOLOGY**

*In*

**VLSI SYSTEM DESIGN**

**By**

**G. PAVANI (17E11D5706)**

*Under the Guidance of*

**Mr. BASAVARAJU**

**Asst. Professor, ECE.**


**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**

**(Approved by AICTE &Affiliated to JNTUH) Mangalpally, Ibrahimpatnam, R.R Dist.-501510, T.S**

**2017-2019**

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**
**MANGALPALLY, IBRAHIMPATNAM, R.R DIST -501510, T.S**
**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**


# CERTIFICATE

This is to certify that the project word titled **"IMPLEMENTATION OF HIGH SPEED VEDIC MULTIPLIER"** that is being submitted by **G. PAVANI (17E11D5706)** in partial fulfillment of the requirements of the award of **MASTER OF TECHNOLOGY**, is a record of bonafide work done under my guidance. The contents of this project work, in full or in parts, have either been taken from any other Institute or University for award of any degree or diploma and the same is certified.

Internal Guide 21/01/20

Mr.Basavaraju

Asst. Professor


Vaithiam Baby 24/01/2020

HOD

**The thesis is satisfactory/unsatisfactory**

External Examiner

# ABSTRACT

Vedic Mathematics ,the ancient Indian mathematics system rediscovered in the beginning of twentieth century. Multiplication process is lengthy and time-consuming task. Implementation of Vedic multiplication in the programmable gate array field has reduced the amount of steps and circuit delays by large scale. Complementary metal oxide semiconductor (CMOS) logic is often used at the circuit stage to develop Vedic multiplier. The design of high speed Vedic Multiplier using the techniques of Vedic Mathematics that have been modified to improve performance. A simple digital multiplier (referred henceforth as Vedic multiplier) architecture based on the Urdhva Tiryagbhyam (Vertically and Crosswise technique) Sutra is presented. Urdhva Tiryagbhyam is the commonly used sutra for multiplication of decimal numbers, which reduced calculation time. It is applied to the binary number system to make it useful in the digital hardware. Essential requirements(here we are used 130nm technology) of many applications are to reduce the time delays and power utilization. Mentor Graphics, an innovation heard in electronic design automation (EDA) offering both hardware and software solution designs, enabling companies to market better electronic products quickly and cost effective.

# CHAPTER 6
# CONCLISION

f Vedic multipliers using Urdhva Tiryakbhyam Sutra" based on Vedic mathematics
lemented on EDA Tool. The Vedic methods used for the multiplier clearly and
ates the computational. The Vedic methods advantages of the computational
e computation path delay for 4x4 array multiplier was 25.712 ns, and for proposed
ltiplier is found to be 0.40ns by using technology node. Hence it can reduce delay
erefore, we are observes the performance of the 4-bit Vedic multiplier highly
n compared to array multiplier in terms of speed.

# SPEED ALU USING MENTOR GRAPHICS

## A PROJECT REPORT

*Submitted in partial fulfillment of the requirements for the award of the degree of*

**MASTER OF TECHNOLOGY**

***In***

**VLSI SYSTEM DESIGN**

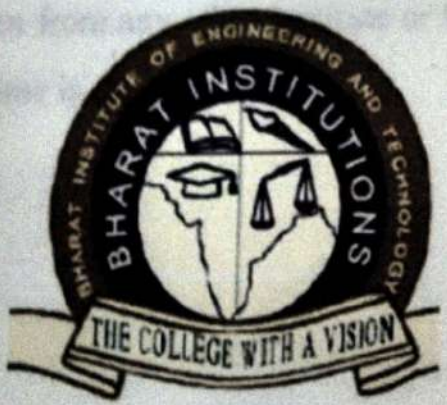
**By**

**R.SHASHIKALA (17E11D5709)**

***Under the Guidance of***

**Mr. D. SANKARA REDDY**

**Asst. Professor, ECE.**




**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**

**(Approved by AICTE &Affiliated to JNTUH) Mangalpally, Ibrahimpatnam, R.R Dist.-501510, T.S**

**2017-2019**

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**
**MANGALPALLY, IBRAHIMPATNAM, R.R DIST -501510, T.S**
**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

# CERTIFICATE

This is to certify that the project word titled **"VLSI IMPLEMENTATION OF ADDERS FOR HIGH SPEED ALU USING MENTOR GRAPHICS"** that is being submitted by **R.SHASHIKALA (17E11D5709)** in partial fulfillment of the requirements of the award of **MASTER OF TECHNOLOGY,** is a record of bonafide work done under my guidance. The contents of this project work, in full or in parts, has either been taken from any other Institute or University for award of any degree or diploma and the same is certified.

D.S

**Internal Guide**
**Mr.D. Sankara Reddy**
**Asst. Professor**

Vth Ram Sahy 24/01/2020

**HOD**

**The thesis is satisfactory/unsatisfactory**

**External Examiner**

# ABSTRACT

The objective of this project is to design high performance arithmetic circuits which are faster and have lower power consumption Low Area required by using the logic family of CMOS Technology.Arithmetic Logical Unit is the very important subsystem in the digital system design .It is a combinational logic unit that performs its arithmetic and logic operations. ALUs of various bit-widths are frequently required in very large-scale integrated circuits (VLSI) from processors to application specific integrated circuits (ASICs).

ALU is getting smaller and more complex nowadays to enable the development of a more powerful but smaller computer. The demand for low power & high speed processing has been increasing as a result of expanding computer and signal processing applications. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications.

In this project, we are going to observe different types of Adders, and will observe the best one to get low delay, less area, low power Consumption and high performance.For example we have many types of Adders like Ripple carry adder(output is known after the carry generated by the previous stage), carry look ahead adder(solves the carry delay in advance, based on the input signal) etc.,

# CHAPTER 6

# CONCLUSION AND FUTURE WORK

Arithmetic Logic Unit is the very important subsystem in the digital system design. In this project, the performances of adder topologies are tested for robustness against area, delay and power dissipation. They are selected for this work since they have been commonly used in many applications. Addition is an indispensable operation for any high speed digital system, digital signal processing or control system. Therefore pertinent choice of adder topologies is an essential importance in the design of VLSI integrated circuits for high speed and high performance CMOS circuits. In this project I have successfully implemented logic gates and adders schematic and layout designing.

By using Mentor graphics EDA tool I checked DRC reports, LVS reports and Parasitic Extraction of the circuits. And also made an observation of the power dissipation, delay, rise time and fall time of logic gates and Adders. From the delay comparison it is observed that the maximum delay occurs for ripple carry adder. The minimum delay occurs for carry select, carry skip adders. The overall comparison presents the tradeoff between area, power dissipation and delay.

According to the presented results, the adder topology which has the best compromise between area, delay and power dissipation are carry look-ahead, suitable for high performance and low-power circuits. The fastest adders are carry select and carry save adders with the penalty of area. The simplest adder topologies that are suitable for low power applications are ripple carry adder, carry skip adder.

# HIGH PERFORMANCE OF 5G SYSTEMS USING MASSIVE MIMO

**A DESSERTATION**

*Submitted in partial fulfillment of the requirements for the award of*

*the degree of*

**MASTER OF TECHNOLOGY**

*in*

**WIRELESS AND MOBILE COMMUNICATION**

By

**SNEHA MERIN PHILIP (16E11D6501)**

*Under the Guidance of*

**Dr. NAVEEN RATHEE**

**Professor, ECE.**


DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**

(Approved by AICTE & Affiliated to JNTUH)

Mangalpally, Ibrahimpatnam, R.R Dist. -501510, T.S

December-2018

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**
MANGALPALLY, IBRAHIMPATNAM, R.R DIST. -501510, T.S

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**


## CERTIFICATE

This is to certify that the dissertation entitled **"HIGH PERFORMANCE OF 5G SYSTEMS USING MASSIVE MIMO"** that is being submitted by SNEHA MERIN PHILIP (Reg. No- 16E11D6501) in partial fulfillment for the award of **Masters of Technology in WIRELESS AND MOBILE COMMUNICATION** in the department of Electronics and Communication Engineering to Jawaharlal Nehru Technological University, Hyderabad is a record of bonafide work carried out by her at our institution Bharat Institute of Engineering And Technology.

13/12/18
**Internal Guide**
**(Dr. NAVEEN RATHEE)**

13/12/18
**M.Tech Coordinator**
**(Mr. V. PRADEEP KUMAR)**

13/12/18
**Academic Incharge**
**(Dr. NEERAJ MISHRA)**

**The thesis is satisfactory/unsatisfactory.**

**External Examiner**

# ABSTRACT

Massive MIMO (multiple-input multiple-output)antenna technology can provide significant performance improvement for cellular systems in terms of both throughput and energy efficiency. It is widely recognized that inter-user interference can be eliminated with a large number of antennas because of the asymptotical orthogonality among users when linear MF (Matched Filter) downlink precoding is used in the NodeB. Due to the complexity and deployment consideration in practical scenarios at individual eNodeBs, cooperative massive MIMO [CM-MIMO] where multiple base stations cooperate together and form a distributed antenna array to serve multiple users simultaneously is an attractive alternative. Furthermore, cooperative massive MIMO can also help increase the system performance especially for cell edge users because of the cooperative transmission among neighboring cells. In this paper, system level simulation performance for the downlink, based upon current LTE systems, provides an indication of the achievable potential system performance improvement by employing CM-MIMO in future (5G) cellular networks. It is demonstrated that CM-MIMO can improve the system performance of cell edge users significantly even if the cell average performance is very slightly degraded or maintained caused by the power imbalance of received signal from different cooperative neighboring cells.

# CHAPTER 7

# CONCLUSION AND FUTURE SCOPE

## 7.1. CONCLUSION

In this venture, framework level recreation execution of non-helpful and agreeable gigantic MIMO frameworks for downlink execution is introduced in view of current LTE frameworks considering diverse quantities of receiving wires conveyed in the base station. It is demonstrated that through collaboration among base stations, framework execution of cell edge clients can be fundamentally enhanced, while cell normal throughput is somewhat debased or kept up inferable from the power lopsidedness for the cell focus clients. The framework reenactments displayed in this proposal give a perspective of the potential framework execution that can be accomplished by agreeable gigantic MIMO advances in down to earth 5G frameworks. Future research will be on framework execution assessment of helpful monstrous MIMO just for cell focus clients too.

# ADVANCE CO-EXISTENCE SYSTEM OF LONG TERM EVOLUTION RELEVANCES

*Submitted in partial fulfillment of the requirements for the award of*

*the degree of*

**MASTER OF TECHNOLOGY**

*In*

**WIRELESS AND MOBILE COMMUNICATION**

By

**CHERUKUPALLI SAI BHARGAV (16E11D6502)**

*Under the Guidance of*

**Dr. RAMBABU VATTI**

**Professor, ECE.**


DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**

(Approved by AICTE & Affiliated to JNTUH)

Mangalpally, Ibrahimpatnam, R.R Dist. -501510, T.S

December-2018

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**

**MANGALPALLY, IBRAHIMPATNAM, R.R DIST. -501510, T.S**

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

## CERTIFICATE

This is to certify that the dissertation entitled **"ADVANCE CO-EXISTENCE SYSTEM OF LONG TERM EVOLUTION RELEVANCES"** that is being submitted by CHERUKUPALLI SAI BHARGAV (Reg. No- 16E11D6502) in partial fulfillment for the award of **Masters of Technology in WIRELESS AND MOBILE COMMUNICATION** in the department of Electronics and Communication Engineering to Jawaharlal Nehru Technological University, Hyderabad is a record of bonafide work carried out by him at our institution Bharat Institute of Engineering And Technology.

13/12/18

**Internal Guide**

**(Dr. RAMBABU VATTI)**

**PROFESSOR**

V. Pradeep 13/12/18

**M.Tech. Incharge**

**(Mr. V. PRADEEP KUMAR)**

**MTECHCOORDINATOR**

Neeraj 13/12/18

**Academic Incharge**

**(Dr. NEERAJ MISRA)**

The thesis is satisfactory/unsatisfactory.

A. Bhagavathi

**External Examiner**

# ABSTRACT

Due to the increasing demand for higher data rates and the congestion in communication systems, new research is focusing on the cooperation between the two most successful communication systems, LTE and Wi-Fi. The overall performance of a Wi-Fi system degrades with increasing the number of served users due to collisions. We propose in this paper a novel scheme for LTE and Wi-Fi coexistence, where an LTE femto Base Station cooperates with a Wi-Fi Access Point to maximize both of their profits. Our proposed scheme has the advantage of relieving a congested Wi-Fi system. Thus, this creates a time gap for the LTE system to transmit its data. In addition, we investigate the capability of Wi-Fi and LTE systems to work simultaneously under a certain maximum interference limit. We have formulated a multi-objective optimization problem for maximizing the rate of the Wi-Fi system and the capacity of the LTE system. We developed an algorithm based on particle swarm optimization to determine the appropriate time ratios for Wi-Fi and LTE transmission, the transmitting power of LTE under Wi-Fi transmission, and the number of Wi-Fi nodes to be transferred to LTE system. Simulation results confirm the capability for LTE to transmit besides Wi-Fi without affecting its transmission rate.

# CHAPTER 8

# CONCLUSION

## Conclusion

In this project, we have discussed the capability of LTE to operate, coherently and fairly, with a nearby Wi-Fi system in the unlicensed band. The LTE system relieves the Wi-Fi system and, thus, gets a dedicated time for its transmission. We have modeled the problem as a two-objective optimization problem. PSO was used for solving the problem and producing the trade-off curve between LTE and Wi-Fi transmission rates. An appropriate point on the curve can be chosen that guarantees the Wi-Fi rate. Simulation results indicated the effectiveness of the proposed cooperative coexistence scheme. The proposed scheme outperforms a previously proposed scheme where the time is divided between the Wi-Fi and LTE systems, by allowing simultaneous transmission of the two systems.

# IDENTIFYING DATA INTERCHANGE FOR COGNITIVE RADIO NETWORKS THROUGH CLAMOR INCONSISTENCY INSECURITY

## A DESSERTATION

*Submitted in partial fulfillment of the requirements for the award of the*

*degree of*

## MASTER OF TECHNOLOGY

*in*

## WIRELESS AND MOBILE COMMUNICATION

By

**E. SUMAKER REDDY (16E11D6504)**

*Under the Guidance of*

**Dr. K. S. BALAMURUGAN**

**Associate Professor, ECE.**

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**

(Approved by AICTE & Affiliated to JNTUH)

Mangalpally, Ibrahimpatnam, R.R Dist. -501510, T.S

December-2018

**BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY**

MANGALPALLY, IBRAHIMPATNAM, R.R DIST. -501510, T.S

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

## CERTIFICATE

This is to certify that the dissertation entitled **"IDENTIFYING DATA INTERCHANGE FOR COGNITIVE RADIO NETWORKS THROUGH CLAMOR INCONSISTANCY INSECURITY"** that is being submitted by E. SUMAKER REDDY (Reg. No- 16E11D6504) in partial fulfillment for the award of **Masters of Technology in WIRELESS AND MOBILE COMMUNICATION** in the department of Electronics and Communication Engineering to Jawaharlal Nehru Technological University, Hyderabad is a record of bonafied work carried out by him at own institution Bharat Institute of Engineering And Technology.

**Internal Guide**

**(Dr. K.S.BALAMURUGAN)**

**M.Tech Co ordinator**

**(Mr. V. PRADEEP KUMAR)**

**Academic Incharge**

**(Dr. NEERAJ MISRA)**

**The thesis is satisfactory /unsatisfactory.**

**External Examiner**

# ABSTRACT

This paper proposes novel spectrum sensing set of rules, and examines the sensing throughput trade off for cognitive radio (CR) networks under noise variance uncertainty. It is assumed that there are one white sub-band, and one goal sub-band that is white or non-white. Under this assumption, first we recommend a unique generalized power detector (GED) for studying the aim sub-band via exploiting the noise records of the white sub-band, then, we've a have a look at the tradeoff among the sensing time and capability throughput of the CR community. To check this tradeoff, we take into account the sensing time optimization for maximizing the throughput of the CR community even as appropriately protective the number one network. The sensing time is optimized via using the derived detection and fake alarm chances of the GED. The proposed GED does now not be stricken via signal to noise ratio (SNR) wall (i.E., robust in opposition to noise variance uncertainty) and outperforms the winning sign detectors. Moreover, the relationship a few of the proposed GED and traditional energy detector (CED) is quantified analytically.

We show that the top-high-quality sensing times with ideal and imperfect noise variances aren't the same. In specific, while the frame period is 2s, SNR= −20dB, and every of the bandwidths of the white and aim sub-bands is 6MHz, the maximum green sensing times are 28.5ms and 50.6ms with perfect and imperfect noise variances, respectively. This correspondence investigates a joint spectrum sensing scheme in cognitive radio networks with unknown and dynamic noise variance. A novel Bayesian solution is proposed to get better the dynamic noise variance and come across the occupancy of primary frequency band simultaneously. The states of number one customers are detected based totally on particle filtering era, after which, the noise parameters are tracked with the resource of using finite dimensional statistics for each particle based totally on marginalized adaptive particle filtering. Simulation outcomes are furnished to validate that the proposed technique can beautify the sensing overall performance significantly and target the dynamic noise variance as it should be.

## CONCLUSION

In this correspondence, we increase a novel SS set of regulations for CR systems with dynamic noise variance. By fully exploiting the dynamic properties of PU country and noise variance, a DSM is formulated and a sequential spectrum scheme is designed via manner of tracking the dynamic noise variance and PU states together. Simulation outcomes were supplied to validate the first-rate sensing overall performance of the proposed set of guidelines.